Software-Defined Radio with PicoZed™ SDR SpeedWay Design Workshops™

Technology Lifecycle

This course will present selected topics in wireless communications with the Avnet PicoZed SDR Software Defined Radio Development Kit. Using system-level design techniques you will model the entire signal chain from RF to baseband within Analog Devices AD9361 agile RF transceiver and Xilinx Zynq All-Programmable SoC.

Hands-on labs will progress though the essential components of modern wireless communication systems using MATLAB® and Simulink® for simulation, code generation and real-time data acquisition with over-the-air testing. You will gain practical experience with tools from Analog Devices, MathWorks and Xilinx to build software-defined radio systems with PicoZed SDR from concept to product deployment.

During this seminar, you will gain insight into

- Avnet PicoZed SDR software-defined radio from concept to deployment
- Model-Based Design using MATLAB and Simulink for simulation, algorithm validation, code generation and over-the-air testing
- Integrating Simulink models into Zynq-based software-defined radio using Xilinx Vivado® Design Suite

Who should attend

- Wireless communications system designers seeking high-level modeling of the entire signal chain from RF to baseband, and code generation for Zynq SoC
- Designers of FPGA-based systems including
  - General purpose software-defined radio
  - Instrumentation (Spectrum Analyzers, Integrated RF Test Solutions)
- Experience in digital signal processing and Xilinx FPGA and Zynq SoC design is recommended but not mandatory

Date/Location:

This two day course will be run in Adelaide on Thursday 24th and Friday 25th of November, 2016.

Ordering Information/Cost:

Ordering Code: **AES-SDRSPWY15-KIT**

Description: Attendance to the 2-Day course plus the PicoZed™ SDR Development Kit

Resale: US$1995 excluding GST and Delivery

Ordering Code: **AES-SDRSPWY15-ATTEND**

Description: Attendance to the 2-Day workshop for customers whom have already purchased the PicoZed SDR kit from Avnet ANZ.

Resale: US$995 excluding GST

Accelerating Your Success™

SpeedWay Agenda Day 1

TYPE	DESCRIPTION
Lecture	**System modeling with PicoZed SDR**
Lab	**Modeling and simulating AD9361 RF transceiver with MATLAB and SimRF** Using a validated SimRF model of the AD9361 transceiver, a Simulink-based test bench will exercise a QPSK link in order to determine the optimal settings to program the AD9361 device on PicoZed SDR for live operation. The effects of nonlinearity, noise, gain and phase imbalance, spectral leakage, and other imperfections introduced by the RF transmitter and receiver within AD9361 will be evaluated. Attendees will learn how to introduce interfering signals and mitigate their effects.
Lecture	**Prototyping and testing with PicoZed SDR** This topic focuses on prototyping with PicoZed SDR for fast proof of concept of wireless communications algorithms using MATLAB and Simulink from MathWorks. System designers will learn to use PicoZed SDR as the RF front-end for over-the-air capture of real-world analog signals for streaming to Simulink over Ethernet using ZynqSDR Support from Communications System Toolbox.
Lab	**QPSK Receiver with Radio-in-the-Loop** A real-time RF signal carrying up-converted QPSK digital modulation will be sent over the air. The RF signal will be captured by AD9361 RF transceiver within PicoZed SDR, down converted to baseband, digitized and the raw digital QPSK signal sent over Ethernet from PicoZed SDR to the PC running MATLAB and Simulink. The Simulink receiver model will de-modulate the QPSK and frame the incoming bitstream to retrieve the payload sent by the transmitter.

SpeedWay Agenda Day 2

TYPE	DESCRIPTION
Lecture	**System integration with PicoZed SDR** This section presents a methodology for integration of wireless communications algorithms into a top-level system for stand-alone operation on PicoZed SDR. System designers will learn how to optimize a Simulink model for efficient hardware implementation in ZynqSoC, then build the entire system using the automation within HDL Workflow Advisor from MathWorks.
Lab	**Integrating QPSK receiver IP into PicoZed SDR with Simulink and Xilinx Vivado Design Suite** Using an automated workflow within Simulink, an IP core will be generated directly from the QPSK receiver model and integrated into a Vivado-based board support package custom-made for PicoZed SDR. The design will be verified in behavioral HDL simulation within Vivado, then compiled to a bitstream and all necessary files created to boot PicoZed SDR for stand-alone operation. Attendees will tune system parameters while in real-time operation through Ethernet connectivity using Simulink external mode.
Lecture	**Product deployment with PicoZed SDR** This lecture demonstrates live usage of PicoZed SDR running UBUNTU Linux desktop on the ARM® Cortex™-A9 processing system (PS) of the Zynq®-7000 All Programmable SoC. Topics include Analog Devices IIO Oscilloscope for display of captured RF-modulated QPSK data in the frequency domain and constellation plot, remote update of user space tools in the Linux root file-system, Zynq Boot Files and Linux kernel in the FAT32 BOOT partition.

For more information please contact: XilinxANZ@avnet.com

CONTACT INFORMATION

Australia

NSW	T +61 (2) 9585 5511
VIC	T +61 (3) 9760 4250
SA	T +61 (8) 8104 5400
QLD	T +61 (7) 3269 3166
WA	T +61 (8) 9301 1500

New Zealand

Auckland	T +64 (9) 914 7900
Christchurch	T +64 (3) 962 0580

Accelerating Your Success™

WWW.EM.AVNETASIA.COM